Amendments to the Claims:

This listing of claims will replace all prior versions, and listing, of claims in the application:

Listing of Claims:

Claim 1 (currently amended): A driver circuit, comprising:

a first current path coupled to a first voltage;

a first switching circuit, under control of an input signal, to couple and uncouple ~~said~~the first current path to an output of the driver circuit;

a first current clamp, coupled in the first current path, to prevent a voltage at ~~said~~the output of the driver circuit from reaching said first voltage;

a delay circuit, coupled to the output of the driver circuit; and

a first non-persistent charge boost circuit, ~~coupled to the first switching circuit,~~ to increase a rate at which ~~said~~the output of the driver circuit switches toward ~~said~~the first voltage when ~~said~~the first current path is coupled to ~~said~~the output of the driver circuit, wherein the charge boost circuit comprises a field effect transistor that is i) coupled in parallel with the first current clamp via its source and drain terminals, and ii) has its gate coupled to an output of the delay circuit.

Claim 2 (original): The driver circuit of claim 1, wherein the first current clamp comprises a resistor.

Claim 3 (original): The driver circuit of claim 2, wherein the first non-persistent charge boost circuit comprises a capacitor, coupled in parallel with said resistor.

Claim 4 (canceled)

Claim 5 (original): The driver circuit of claim 3, further comprising:

a signal line coupled to said output; and

a receiver coupled to said signal line;

wherein said capacitor of the first non-persistent charge boost circuit has a value that is at least twice the sum of i) the capacitance of the signal line, and ii) the gate capacitance of the receiver.

Claim 6 (canceled)

Claim 7 (original): The driver circuit of claim 1, wherein the first switching circuit comprises a field effect transistor, the source and drain of which are coupled in said first current path, and the gate of which receives said input signal.

Claim 8 (original): The driver circuit of claim 1, further comprising:

a signal line coupled to said output;

a receiver coupled to said signal line; and

a voltage clamp, coupled to said signal line in proximity to said receiver, to prevent a voltage at said receiver from reaching said first voltage.

Claim 9 (original): The driver circuit of claim 1, further comprising:

a second current path coupled to a second voltage;

a second switching circuit, under control of said input signal, to couple and uncouple said second current path to said output;

a second current clamp, coupled in the second current path, to prevent a voltage at said output from reaching said second voltage; and

a second non-persistent charge boost circuit, coupled to the second switching circuit, to increase a rate at which said output switches toward said second voltage when said second current path is coupled to said output.

Claim 10 (currently amended): The driver circuit of claim 9, further comprising ~~first and~~a second delay ~~circuits~~circuit, coupled to the output of the driver circuit, wherein:

~~the first non-persistent charge boost circuit comprises a first field effect transistor that is coupled in the first current path via its source and drain terminals;~~

~~the gate of the first field effect transistor is coupled to an output of the first delay circuit;~~

the second non-persistent charge boost circuit comprises a second field effect transistor that is coupled in the second current path via its source and drain terminals; and

the gate of the second field effect transistor is coupled to an output of the second delay circuit.

Claim 11 (currently amended): The driver circuit of claim 9, ~~further comprising a delay circuit, coupled to the output of the driver circuit,~~ wherein:

~~the first non-persistent charge boost circuit comprises a first field effect transistor that is coupled in the first current path via its source and drain terminals;~~

the second non-persistent charge boost circuit comprises a second field effect transistor that is coupled in the second current path via its source and drain terminals; and

the ~~gates~~gate of the ~~first and~~ second field effect ~~transistors are~~transistor is coupled to [[an]]the output of the delay circuit.

Claim 12 (original): The driver circuit of claim 9, further comprising:

a signal line coupled to said output;

a receiver coupled to said signal line; and

first and second voltage clamps, coupled to said signal line in proximity to said receiver, to prevent a voltage at said receiver from reaching either of said first or second voltages.

Claim 13 (original): The driver circuit of claim 1, wherein the first current clamp is coupled to the first non-persistent charge boost circuit to arm the first non-persistent charge boost circuit when the first current path is not coupled to said output.

Claim 14 (currently amended): A driver circuit, comprising:

a first current path coupled to a first voltage;

first switching means to couple and uncouple the first current path to an output of the driver circuit;

first current clamping means, coupled in the first current path, to prevent a voltage at ~~said~~the output of the driver circuit from reaching said first voltage;

delay means, coupled to the output of the driver circuit; and

first non-persistent charge boost means, ~~coupled to the first switching means,~~ to increase a rate at which ~~said~~the output of the driver circuit switches toward ~~said~~the first voltage when ~~said~~the first current path is coupled to ~~said~~the output of the driver circuit, wherein the charge boost means comprises a field effect transistor that is i) coupled in parallel with the first current clamping means via its source and drain terminals, and ii) has its gate coupled to an output of the delay means.

Claim 15 (canceled)

Claim 16 (original): The driver circuit of claim 14, further comprising:

a second current path coupled to a second voltage;

second switching means to alternately couple and uncouple said second current path to said output;

second current clamping means, coupled in the second current path, to prevent a voltage at said output from reaching said second voltage; and

second non-persistent charge boost means, coupled to the second switching means, to increase a rate at which said output switches toward said second voltage when said second current path is coupled to said output.

Claim 17 (currently amended): A method, comprising:

under control of an input signal, driving a signal line toward a first voltage by coupling a first current path to the signal line;

while the first current path is coupled to the signal line,

i) clamping current flow through the signal line, by means of a series-connected resistor in the first current path, to prevent the voltage on the signal line from reaching the first voltage; and

ii) providing a non-persistent charge boost to the signal line, by means of a field effect transistor that is i) coupled in parallel with said resistor via its source and drain terminals, and ii) has a gate that is driven by a delayed version of the voltage on the signal line, to increase a rate at which a voltage on the signal line switches toward said first voltage~~; and~~

~~ii) clamping current flow through the signal line to prevent said voltage on said signal line from reaching said first voltage~~.

Claim 18 (original): The method of claim 17, further comprising clamping voltages at a receiving end of the signal line to a range of voltages that is smaller than a range of voltages allowed at a driven end of the signal line.

Claim 19 (original): The method of claim 17, further comprising:

under control of said input signal, driving said signal line toward a second voltage by uncoupling the first current path from the signal line and coupling a second current path to the signal line;

while the second current path is coupled to the signal line,

i) providing a non-persistent charge boost to the signal line, to increase a rate at which the voltage on the signal line switches toward said second voltage; and

ii) clamping current flow through the signal line to prevent a voltage on said signal line from reaching said second voltage.

Claim 20 (original): The method of claim 19, further comprising clamping voltages at a receiving end of the signal line to a range of voltages that is smaller than a range of voltages allowed at a driven end of the signal line.

Claim 21 (original): The method of claim 17, wherein, when the first current path is uncoupled from the signal line, the method used to clamp current provides a means to arm the charge boost.

Claim 22 (canceled)

Claim 23 (currently amended): The method of claim 22, wherein said non-persistent charge boost is further provided by a capacitor, coupled in parallel with said resistor.

Claim 24 (canceled)